



IN THE UNITED STATES PATENT AND TRADEMARK OFFICE  
(Case No. RA043D2C3C2)

the Application of:

FARMWALD ET AL.

Serial No: 09/779,296

Filed: February 8, 2001

Title: MEMORY DEVICE HAVING A  
VARIABLE DATA OUTPUT LENGTH

Assistant Commissioner for Patents  
Washington, DC 20231

Group Art Unit: 2818

Before

Examiner: T. Nguyen

INFORMATION DISCLOSURE STATEMENT

Dear Sir:

The documents listed in the PTO-1449 are documents which were cited and provided in a parent application of the above-referenced application, namely Application Serial No. 09/492,982, filed January 27, 2000. Pursuant to 37 C.F.R. §1.98(d) and M.P.E.P. §609, copies of the documents listed in the modified Form PTO-1449 are not provided herewith.

It is believed that the Examiner may find the documents cited in the modified Form PTO-1449 material to the patentability of one or more of the claims in the above-captioned application. Accordingly, it is respectfully requested that the Examiner make his consideration of these references formally of record with the initial Office Action.

Respectfully submitted,

Date: May 1, 2001

Neil A. Steinberg  
Reg. No. 34,735  
650-947-5325

4/20/01  
S. Mackey  
7-7-01



PTO-1449 (Modified)  U.S. DEPARTMENT OF COMMERCE PATENT AND TRADEMARK OFFICE  INFORMATION DISCLOSURE STATEMENT BY APPLICANT	ATTY. DOCKET NO. RA043D2C3C2	SERIAL NUMBER 09/779,296
	APPLICANT(S)  FARMWALD ET AL.	
	FILING DATE FEBRUARY 8, 2001	GROUP ART UNIT 2818

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	4,792,926	12/20/88	Roberts			
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	H. L. Kalter et al. "A 50-ns 16Mb DRAM with a 10-ns Data Rate and On-Chip ECC", IEEE Journal of Solid State Circuits, vol. 25 No. 5, pp. 1118-1128 (Oct 1990)
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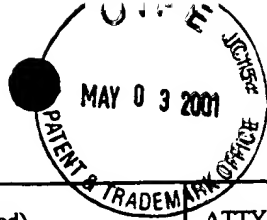
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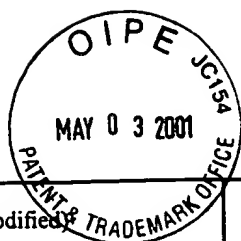
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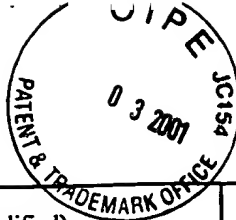
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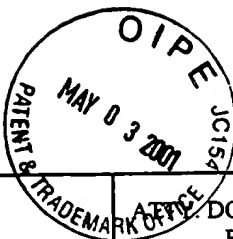
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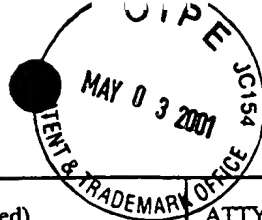
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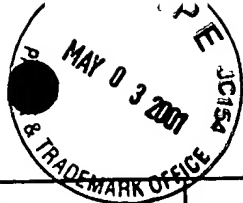
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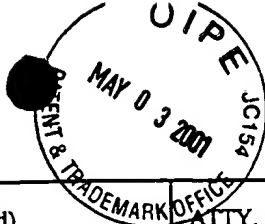
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	FILING DATE FEBRUARY 8, 2001	GROUP ART UNIT 2818

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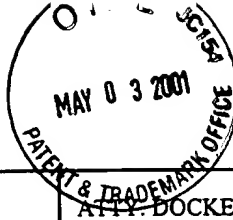
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